Predictable Out-of-order Execution Using Virtual Traces

Jack Whitham and Neil Audsley

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http://www.jwhitham.org.uk/c/vt.html
Topics in this talk

1. General issues with state-of-the-art worst case execution time (WCET) analysis.
2. Problem: design a CPU to reduce the WCET of a task.
3. Traces; a solution.
4. Virtual traces; a further improvement.
5. Experiments, results, observations.
6. Data scratchpads; a problem.
7. Conclusion.
State-of-the-art WCET analysis

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- Model interactions between code and CPU hardware features.
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![Diagram of Task Execution]

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  - This is the focus of my talk; examples include:
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    - cache modeling
      *e.g.* determine how often a load operation \( X \) “hits”
    - pipeline modeling
      *e.g.* determine the worst-case state of the pipeline at point \( Y \)
State-of-the-art WCET analysis

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- The *timing anomaly problem* makes it impossible to determine which hardware state leads to a greater execution time.

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**Timing anomaly:** A locally smaller WCET may lead to a globally greater WCET.

Solutions do exist for all of these problems, but they (1) raise the engineering cost and/or (2) increase the WCET.
A new sort of solution

Suppose we can replace the CPU with a new (or updated) design, aiming to (1) support WCET analysis, and (2) allow the WCET to be reduced.

How could WCET analysis be supported?
Allow the CPU behavior to be safely captured by measurement.
Not usually possible in current CPUs, since there are too many factors affecting timing, and the CPU can't be forced into a known state.
Constrain/isolate some parts of the design to simplify modeling by reducing possible interactions.

How could the WCET be reduced?
Accommodate speculative and superscalar out-of-order operation so that throughput can be increased versus a simple CPU.
Reduce pessimism in the WCET model.
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- Reduce pessimism in the WCET model.
One possibility: a trace

A trace is a path through a program, chosen to reduce $C$, the worst-case execution time.
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How does this help?

If a program is composed of *traces*, analysis can ignore *how* a computation is performed by the CPU, and instead consider only one thing:

The length of time taken for each path through each trace.

If a trace contains $n$ branches, then there are $n + 1$ paths through it.

$\Rightarrow$ There are exactly $n + 1$ ways that it could ever be executed.

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The trace begins and ends in a known pipeline state. The total time for each path is exactly known (it can be measured). The result: speculation and superscalar out-of-order execution don’t have to be modeled!
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**The result:** speculation and superscalar out-of-order execution don’t have to be modeled!
Contrast with *static branch prediction*. With a virtual trace, the main path has a well-defined end point, so the number of possible pipeline states is *bounded*. Static branch prediction omits this important restriction.
Previous work

In previous work, we considered the use of a *trace scratchpad* to implement traces and meet the requirements, used as follows:

1. Take a program in machine code form;

\[\begin{array}{c}
\text{trace entrance} \\
\text{trace exit} \\
\text{trace exit} \\
\text{trace implemented using microcode} \\
\text{trace} \\
\text{BB4} \\
\text{BB5} \text{BB2} \\
\text{BB3} \text{BB1} \\
\text{BB6} \\
\text{BB1,3,6} \\
\text{BB4} \\
\text{BB5} \text{BB2} \\
\text{(a) (b)} \\
\text{microcode}
\end{array}\]
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1. Take a program in machine code form;
2. Apply WCET analysis to find the WCEP;
3. Convert subsequences of the WCEP into traces implemented by microcode. These are explicitly parallel and optimize execution for one path.
4. Allocate space in a **trace scratchpad** for microcode. The microcode is used in place of the original machine code.

Virtual trace

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- the need for a custom CPU with a writable microcode store,
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- the memory space requirements of microcode.
Virtual trace

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We regard the CPU dynamic scheduler as a decoder:

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*Virtual* in the sense that the microcode is generated dynamically - we know what the scheduler will do, but we don’t explicitly encode it.

RTS York
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1. **Problem:** Pipeline components can interact.

   - **Solution:** Constrain execution to a known state at the beginning and end of each trace. The effects of all interactions are captured when the virtual trace execution time is measured.
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3. **Problem:** Timing anomalies can occur in complex CPUs.
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Statement, research questions

If a program runs using virtual traces, and program functionality can be modeled, then an exact bound for the WCET $C$ can be found.

Q1: Given a task $T$, is $C$ lower if (a) a simple in-order CPU is used (minimum one CPI), or (b) a virtual trace CPU is used.

Q2: Which of the constraints needed to implement virtual traces have the greatest effect on execution time?
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- Virtual traces are implemented using the M5 O3 CPU simulator.

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- Virtual traces are assigned to a single-path program using profiling.
  - In reality, WCET analysis would be used.
  - Chicken and egg problem!

How virtual traces are implemented

(1) Sources of *timing noise* in O3 are constrained or eliminated:

- Instructions
- Instruction Cache Stall
- *virtual trace* Predictions

---

Dynamic Scheduler

- Memory Dependence Misprediction Detected
- Data Cache Stall
- Misprediction Detected
- Exception Detected
- Variable Duration Instruction

---

Instruction interface

- Load/store unit
- Execution unit
How virtual traces are implemented

(2) The *virtual trace controller* (VTC) generates branch predictions and manages the flow of instructions into the pipeline:

Result: O3+VTC CPU: O3 with virtual trace extensions.
Experiment 1

Q1: Given a task $T$, is $C$ lower if
(a) a simple in-order CPU is used (minimum one CPI), or
(b) a virtual trace CPU is used.

A subset of the Mälardalen benchmarks were executed within the following environments, measuring execution time:

- **IIO**: Idealized in-order CPU.  
  *Exactly one instruction executed every clock cycle.*
- **O3+VTC**: Virtual trace CPU with maximum trace length $L \in [1, 20]$.  

*RTS* York
Results 1

O3+VTC: Some WCET reduction achieved for 14 of 17 cases, up to 2.5×.

<table>
<thead>
<tr>
<th></th>
<th>IIO</th>
<th>O3+VTC</th>
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<tbody>
<tr>
<td>bs</td>
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<td>79</td>
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<td>bubble</td>
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<tr>
<td>ns</td>
<td>2,852</td>
<td>1,691</td>
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</tbody>
</table>

Trace length $L$
O3+VTC: Some WCET reduction achieved for 14 of 17 cases, up to $2.5\times$.

But available WCET reductions are highly dependent on program structure; unpredictable branches are a problem. *If-conversion* is a solution (localized single-path programming).
Q2: Which of the constraints needed to implement virtual traces have the greatest effect on execution time?

A subset of the Mälardalen benchmarks were executed within the following environments, measuring execution time. Each environment removes one of the constraints of O3+VTC:

- **O3+VTC-SYNC**: The pipeline is not resynchronized at trace end.
- **O3+VTC-SYNC-IOB**: Branches may be executed out of order.
- **O3+VTC-SYNC-SD**: Dynamic memory disambiguation is used.
- **O3+VTC-SYNC-NF**: Dynamic memory forwarding is permitted.
Unpredictable branches are only one problem! CPU constraints also increase $C$: O3+VTC is up to 3.6× slower than O3.
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In terms of $C$, the most severe constraints are those preventing dynamic memory *disambiguation* and *forwarding*. 

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<table>
<thead>
<tr>
<th>Throughput Increase</th>
<th>Frequency</th>
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<tbody>
<tr>
<td>0</td>
<td>1</td>
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<tr>
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**Legend**

- O3+VTC-SYNC-NF
- O3+VTC-SYNC-SD
- O3+VTC-SYNC-IOB
- O3+VTC-SYNC
Unpredictable branches are only one problem! CPU constraints also increase $C$: O3+VTC is up to $3.6 \times$ slower than O3.

In terms of $C$, the most severe constraints are those preventing dynamic memory *disambiguation* and *forwarding*.

If only we could predict the addresses of loads and stores!
Further Investigation

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  - Q2: How often should the partition be changed?

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Further Investigation

In fact, the memory addresses used for data accesses have an even more significant effect on performance, because of the time taken to fetch data.

- **This work assumed a perfect data cache.** A real data cache would be a source of timing noise; this would be a severe problem. Every hit/miss needs to be predicted in advance.
- A scratchpad memory or locked cache would need to be used. Automatic data scratchpad allocation is necessary but difficult.
  - Q1: Which variables should be stored in scratchpad? Which should be stored in main memory?
  - Q2: How often should the partition be changed?

A hard problem for general C code:

- Pointers can have almost any value.
- Memory might be allocated dynamically.

The same problems affect data cache modeling.
Further Investigation

A solution for automatic data scratchpad allocation would also relax the constraints on dynamic data accesses, because:

- The range of addresses for each data access would be known, so dynamic disambiguation would be unnecessary.
- However, this is not an easy problem.
- Existing automatic data scratchpad allocation systems assume no pointers (global/stack arrays only).
- Other solutions assume an unconventional program paradigm (e.g. dataflow/actor-oriented model).
- The problem needs to be solved for typical C programs; otherwise, assumptions such as “perfect data cache” (as made in this work) will continue to be unrealistic.
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- The CPU constraints reduce the maximum performance but increase the guaranteed performance.
- Predictable management of data accesses is a problem that saps the performance of virtual traces.
- The automatic data scratchpad allocation problem must be solved.
All questions and comments are welcome!

You can find the O3+VTC experimental software on the web at http://www.jwhitham.org.uk/c/vt.html